



D8748H/D8749H HMOS-E SINGLE-COMPONENT 8-BIT MICROCONTROLLER

- High Performance HMOS-E
- Interval Timer/Event Counter
- Two Single Level Interrupts
- Single 5-Volt Supply
- Over 96 Instructions; 90% Single Byte
- Compatible with 8080/8085 Peripherals
- Easily Expandable Memory and I/O
- Up to 1.35 μ s Instruction Cycle;
All Instructions 1 or 2 Cycles

The Intel D8749H/D8748H are totally self-sufficient, 8-bit parallel computers fabricated on single silicon chips using Intel's advanced N-channel silicon gate HMOS-E process.

The family contains 27 I/O lines, an 8-bit timer/counter, on-chip RAM and on-board oscillator/clock circuits. For systems that require extra capability, the family can be expanded using MCS[®]-80/MCS[®]-85 peripherals.

These microcomputers are designed to be efficient controllers as well as arithmetic processors. They have extensive bit handling capability as well as facilities for both binary and BCD arithmetic. Efficient use of program memory results from an instruction set consisting mostly of single byte instructions and no instructions over 2 bytes in length.

| Device | Internal Memory | |
|--------|-----------------|-------------|
| D8749H | 2K x 8 EPROM | 128 x 8 RAM |
| D8748H | 1K x 8 EPROM | 64 x 8 RAM |

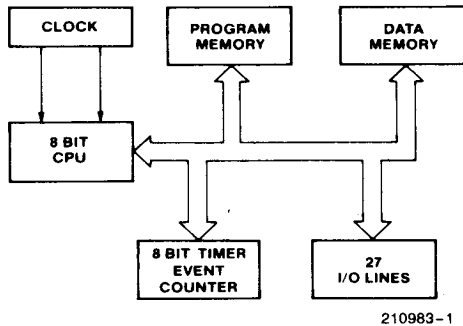


Figure 1.
Block Diagram

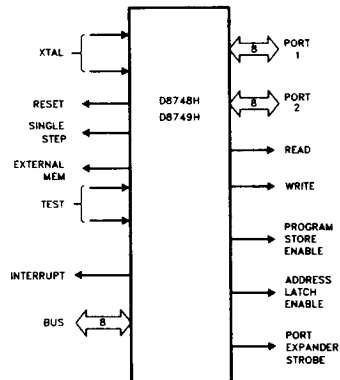
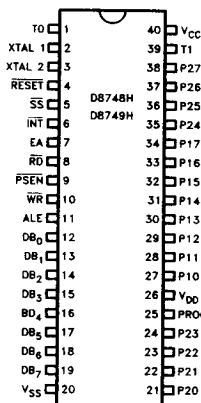


Figure 2.
Logic Symbol



210983-3

Figure 3. Pin Configuration

Table 1. Pin Description (40-Pin DIP)

| Symbol | Pin No. | Function |
|-------------------|---------|--|
| V _{SS} | 20 | Circuit GND potential. |
| V _{DD} | 26 | + 5V during normal operation. |
| | | Programming power supply (+ 21V). |
| V _{CC} | 40 | Main power supply; + 5V during operation and programming. |
| PROG | 25 | Output strobe for 8243 I/O expander. |
| | | Program pulse (+ 18V) input pin during programming. |
| P10–P17 Port 1 | 27–34 | 8-bit quasi-bidirectional port. |
| P20–P23 | 21–24 | 8-bit quasi-bidirectional port. P20–P23 contain the four high order program counter bits during an external program memory fetch and serve as a 4-bit I/O expander bus for 8243. |
| P24–P27 Port 2 | 35–38 | |
| DB0–DB7 BUS | 12–19 | True bidirectional port which can be written or read synchronously using the RD, WR strobes. The port can also be statically latched. Contains the 8 low order program counter bits during an external program memory fetch, and receives the addressed instruction under the control of PSEN. Also contains the address and data during an external RAM data store instruction, under control of ALE, RD, and WR. |
| T0 | 1 | Input pin testable using the conditional transfer instructions JT0 and JNT0. T0 can be designated as a clock output using ENT0 CKL instruction. |
| | | Used during programming. |
| T1 | 39 | Input pin testable using the JT1, and JNT1 instructions. Can be designated the timer/counter input using the STRT CNT instruction. |
| INT | 6 | Interrupt input. Initiates an interrupt if interrupt is enabled. Interrupt is disabled after a reset. Also testable with conditional jump instruction. (Active low) interrupt must remain low for at least 3 machine cycles for proper operation. |
| RD | 8 | Output strobe activated during a BUS read. Can be used to enable data onto the bus from an external device. |
| | | Used as a read strobe to external data memory. (Active low) |

Table 1. Pin Description (40-Pin DIP) (Continued)

| Symbol | Pin No. | Function |
|--------|---------|---|
| RESET | 4 | Input which is used to initialize the processor. (Active low) (Non TTL V_{IH}) |
| | | Used during programming. |
| WR | 10 | Output strobe during a bus write. (Active low) Used as write strobe to external data memory. |
| ALE | 11 | Address latch enable. This signal occurs once during each cycle and is useful as a clock output. The negative edge of ALE strobes address into external data and program memory. |
| PSEN | 9 | Program store enable. This output occurs only during a fetch to external program memory. (Active low.) |
| SS | 5 | Single step input can be used in conjunction with ALE to "single step" the processor through each instruction. |
| EA | 7 | External access input which forces all program memory fetches to reference external memory. Useful for emulation and debug. (Active high.) |
| | | Used during (18V) programming. |
| XTAL1 | 2 | One side of crystal input for internal oscillator. Also input for external source. (Non TTL V_{IH} .) |
| XTAL2 | 3 | Other side of crystal input. |

Table 2. Instruction Set

| Mnemonic | Description | Bytes | Cycles | Mnemonic | Description | Bytes | Cycles |
|--------------------|-------------------------------|-------|--------|--------------------------------|------------------------------|-------|--------|
| ACCUMULATOR | | | | ACCUMULATOR (Continued) | | | |
| ADD A, R | Add register to A | 1 | 1 | INC A | Increment A | 1 | 1 |
| ADD A, @R | Add data memory to A | 1 | 1 | DEC A | Decrement A | 1 | 1 |
| ADD A, #data | Add immediate to A | 2 | 2 | CLR A | Clear A | 1 | 1 |
| ADDC A, R | Add register with carry | 1 | 1 | CPL A | Complement A | 1 | 1 |
| ADDC A, @R | Add data memory with carry | 1 | 1 | DA A | Decimal adjust A | 1 | 1 |
| ADDC A, #data | Add immediate with carry | 2 | 2 | SWAP A | Swap nibbles of A | 1 | 1 |
| ANL A, R | And register to A | 1 | 1 | RL A | Rotate A left | 1 | 1 |
| ANL A, @R | And data memory to A | 1 | 1 | RLC A | Rotate A left through carry | 1 | 1 |
| ANL A, #data | And immediate to A | 2 | 2 | RR A | Rotate A right | 1 | 1 |
| ORL A, R | Or register to A | 1 | 1 | RRC A | Rotate A right through carry | 1 | 1 |
| ORL A, @R | Or data memory to A | 1 | 1 | INPUT/OUTPUT | | | |
| ORL A, #data | Or immediate to A | 2 | 2 | IN A, P | Input port to A | 1 | 2 |
| XRL A, R | Exclusive or register to A | 1 | 1 | OUTL P, A | Output A to port | 1 | 2 |
| XRL A, @R | Exclusive or data memory to A | 1 | 1 | ANL P, #data | And immediate to port | 2 | 2 |
| XRL A, #data | Exclusive or immediate to A | 2 | 2 | ORL P, #data | Or immediate to port | 2 | 2 |
| | | | | INS A, BUS | Input BUS to A | 1 | 2 |
| | | | | OUTL BUS, A | Output A to BUS | 1 | 2 |
| | | | | ANL BUS, #data | And immediate to BUS | 2 | 2 |
| | | | | ORL BUS, #data | Or immediate to BUS | 2 | 2 |
| | | | | MOVD A, P | Input expander port to A | 1 | 2 |

Table 2. Instruction Set (Continued)

| Mnemonic | Description | Bytes | Cycles |
|---------------------------------|-----------------------------|-------|--------|
| INPUT/OUTPUT (Continued) | | | |
| MOVD P, A | Output A to expander port | 1 | 2 |
| ANLD P, A | And A to expander port | 1 | 2 |
| ORLD P, A | Or A to expander port | 1 | 2 |
| REGISTERS | | | |
| INC R | Increment register | 1 | 1 |
| INC @R | Increment data memory | 1 | 1 |
| DEC R | Decrement register | 1 | 1 |
| BRANCH | | | |
| JMP addr | Jump unconditional | 2 | 2 |
| JMPP @A | Jump indirect | 1 | 2 |
| DJNZ R, addr | Decrement register and skip | 2 | 2 |
| JC addr | Jump on carry = 1 | 2 | 2 |
| JNC addr | Jump on carry = 0 | 2 | 2 |
| JZ addr | Jump on A zero | 2 | 2 |
| JNZ addr | Jump on A not zero | 2 | 2 |
| JT0 addr | Jump on T0 = 1 | 2 | 2 |
| JNT0 addr | Jump on T0 = 0 | 2 | 2 |
| JT1 addr | Jump on T1 = 1 | 2 | 2 |
| JNT1 addr | Jump on T1 = 0 | 2 | 2 |
| JF0 addr | Jump on F0 = 1 | 2 | 2 |
| JF1 addr | Jump on F1 = 1 | 2 | 2 |
| JTF addr | Jump on timer flag | 2 | 2 |
| JNI addr | Jump on INT = 0 | 2 | 2 |
| JBb addr | Jump on accumulator bit | 2 | 2 |
| SUBROUTINE | | | |
| CALL addr | Jump to subroutine | 2 | 2 |
| RET | Return | 1 | 2 |
| RETR | Return and restore status | 1 | 2 |
| FLAGS | | | |
| CLR C | Clear carry | 1 | 1 |
| CPL C | Complement carry | 1 | 1 |
| CLR F0 | Clear flag 0 | 1 | 1 |
| CPL F0 | Complement flag 0 | 1 | 1 |
| CLR F1 | Clear flag 1 | 1 | 1 |
| CPL F1 | Complement flag 1 | 1 | 1 |
| DATA MOVES | | | |
| MOV A, R | Move register to A | 1 | 1 |
| MOV A, @R | Move data memory to A | 1 | 1 |
| MOV A, #data | Move immediate to A | 2 | 2 |

| Mnemonic | Description | Bytes | Cycles |
|-------------------------------|-----------------------------------|-------|--------|
| DATA MOVES (Continued) | | | |
| MOV R, A | Move A to register | 1 | 1 |
| MOV @R, A | Move A to data memory | 1 | 1 |
| MOV R, #data | Move immediate to register | 2 | 2 |
| MOV @R, #data | Move immediate to data memory | 2 | 2 |
| MOV A, PSW | Move PSW to A | 1 | 1 |
| MOV PSW, A | Move A to PSW | 1 | 1 |
| XCH A, R | Exchange A and register | 1 | 1 |
| XCH A, @R | Exchange A and data memory | 1 | 1 |
| XCHD A, @R | Exchange nibble of A and register | 1 | 1 |
| MOVX A, @R | Move external data memory to A | 1 | 2 |
| MOVX @R, A | Move A to external data memory | 1 | 2 |
| MOVP A, @A | Move to A from current page | 1 | 2 |
| MOVP3 A, @A | Move to A from page 3 | 1 | 2 |
| TIMER/COUNTER | | | |
| MOV A, T | Read timer/counter | 1 | 1 |
| MOV T, A | Load timer/counter | 1 | 1 |
| STRT T | Start timer | 1 | 1 |
| STRT CNT | Start counter | 1 | 1 |
| STOP TCNT | Stop timer/counter | 1 | 1 |
| EN TCNTI | Enable timer/counter interrupt | 1 | 1 |
| DIS TCNTI | Disable timer/counter interrupt | 1 | 1 |
| CONTROL | | | |
| EN I | Enable external interrupt | 1 | 1 |
| DIS I | Disable external interrupt | 1 | 1 |
| SEL RB0 | Select register bank 0 | 1 | 1 |
| SEL RB1 | Select register bank 1 | 1 | 1 |
| SEL MB0 | Select memory bank 0 | 1 | 1 |
| SEL MB1 | Select memory bank 1 | 1 | 1 |
| ENT0 CLK | Enable clock output on T0 | 1 | 1 |
| NOP | No operation | 1 | 1 |

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias 0°C to +70°C
 Storage Temperature -65°C to +150°C
 Voltage On Any Pin With Respect
 to Ground -0.5V to +7V
 Power Dissipation 1.0 Watt

NOTICE: This is a production data sheet. The specifications are subject to change without notice.

***WARNING:** Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.

DC CHARACTERISTICS $T_A = 0^\circ\text{C to } +70^\circ\text{C}; V_{CC} = V_{DD} = 5V \pm 10\%; V_{SS} = 0V$

| Symbol | Parameter | Limits | | | Unit | Test Conditions | Device |
|-------------------|---|--------|-----|----------|---------------|---|--------|
| | | Min | Typ | Max | | | |
| V_{IL} | Input Low Voltage (All Except RESET, X1, X2) | -0.5 | | 0.8 | V | | All |
| V_{IL1} | Input Low Voltage (RESET, X1, X2) | -0.5 | | 0.6 | V | | All |
| V_{IH} | Input High Voltage (All Except XTAL1, XTAL2, RESET) | 2.0 | | V_{CC} | V | | All |
| V_{IH1} | Input High Voltage (X1, X2, RESET) | 3.8 | | V_{CC} | V | | All |
| V_{OL} | Output Low Voltage (BUS) | | | 0.45 | V | $I_{OL} = 2.0 \text{ mA}$ | All |
| V_{OL1} | Output Low Voltage (RD, WR, PSEN, ALE) | | | 0.45 | V | $I_{OL} = 1.8 \text{ mA}$ | All |
| V_{OL2} | Output Low Voltage (PROG) | | | 0.45 | V | $I_{OL} = 1.0 \text{ mA}$ | All |
| V_{OL3} | Output Low Voltage (All Other Outputs) | | | 0.45 | V | $I_{OL} = 1.6 \text{ mA}$ | All |
| V_{OH} | Output High Voltage (BUS) | 2.4 | | | V | $I_{OH} = -400 \mu\text{A}$ | All |
| V_{OH1} | Output High Voltage (RD, WR, PSEN, ALE) | 2.4 | | | V | $I_{OH} = -100 \mu\text{A}$ | All |
| V_{OH2} | Output High Voltage (All Other Outputs) | 2.4 | | | V | $I_{OH} = -40 \mu\text{A}$ | All |
| I_{L1} | Leakage Current (T1, INT) | | | ± 10 | μA | $V_{SS} \leq V_{IN} \leq V_{CC}$ | All |
| I_{L11} | Input Leakage Current (P10-P17, P20-P27, EA, SS) | | | -500 | μA | $V_{SS} + 0.45 \leq V_{IN} \leq V_{CC}$ | All |
| I_{L12} | Input Leakage Current RESET | -10 | | -300 | μA | $V_{SS} \leq V_{IN} \leq 3.8V$ | All |
| I_{L0} | Leakage Current (BUS, T0) (High Impedance State) | | | ± 10 | μA | $V_{SS} \leq V_{IN} \leq V_{CC}$ | All |
| $I_{DD} + I_{CC}$ | Total Supply Current* | | 80 | 100 | mA | | 8748H |
| | | | 95 | 110 | mA | | 8749H |

NOTE:

* $I_{CC} + I_{DD}$ is measured with all outputs disconnected; SS, RESET, and INT equal to V_{CC} ; EA equal to V_{SS} .

AC CHARACTERISTICS $T_A = 0^\circ\text{C to } +70^\circ\text{C}; V_{CC} = V_{DD} = 5V \pm 10\%; V_{SS} = 0V$

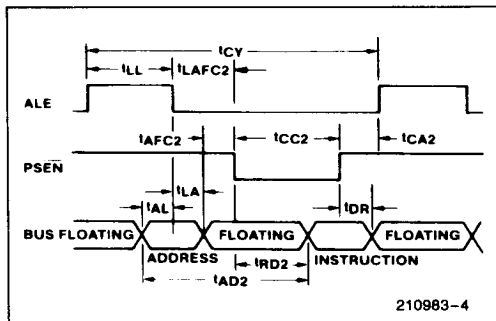
| Symbol | Parameter | f(t) (Note 3) | 11 MHz | | Unit | Conditions (Note 1) |
|--------------------|-------------------------------|------------------|--------|------|------|------------------------|
| | | | Min | Max | | |
| t | Clock Period | 1/xtal freq | 90.9 | 1000 | ns | (Note 3) |
| t _{LL} | ALE Pulse Width | 3.5t – 170 | 150 | | ns | |
| t _{AL} | Addr Setup to ALE | 2t – 110 | 70 | | ns | (Note 2) |
| t _{LA} | Addr Hold from ALE | t – 40 | 50 | | ns | |
| t _{CC1} | Control Pulse Width (RD, WR) | 7.5t – 200 | 480 | | ns | |
| t _{CC2} | Control Pulse Width (PSEN) | 6t – 200 | 350 | | ns | |
| t _{DW} | Data Setup before WR | 6.5t – 200 | 390 | | ns | |
| t _{WD} | Data Hold after WR | t – 50 | 40 | | ns | |
| t _{DR} | Data Hold (RD, PSEN) | 1.5t – 30 | 0 | 110 | ns | |
| t _{RD1} | RD to Data In | 6t – 170 | | 375 | ns | |
| t _{RD2} | PSEN to Data In | 4.5t – 170 | | 240 | ns | |
| t _{AW} | Addr Setup to WR | 5t – 150 | 300 | | ns | |
| t _{AD1} | Addr Setup to Data (RD) | 10.5t – 220 | | 730 | ns | |
| t _{AD2} | Addr Setup to Data (PSEN) | 7.5t – 200 | | 460 | ns | |
| t _{AFC1} | Addr Float to RD, WR | 2t – 40 | 140 | | ns | (Note 2) |
| t _{AFC2} | Addr Float to PSEN | 0.5t – 40 | 10 | | ns | (Note 2) |
| t _{LAFC1} | ALE to Control (RD, WR) | 3t – 75 | 200 | | ns | |
| t _{LAFC2} | ALE to Control (PSEN) | 1.5t – 75 | 60 | | ns | |
| t _{CA1} | Control to ALE (RD, WR, PROG) | t – 65 | 25 | | ns | |
| t _{CA2} | Control to ALE (PSEN) | 4t – 70 | 290 | | ns | |
| t _{CP} | Port Control Setup to PROG | 1.5t – 80 | 50 | | ns | |
| t _{PC} | Port Control Hold to PROG | 4t – 260 | 100 | | ns | |
| t _{PR} | PROG to P2 Input Valid | 8.5t – 120 | | 650 | ns | |
| t _{PF} | Input Data Hold from PROG | 1.5t | 0 | 140 | ns | |
| t _{DP} | Output Data Setup | 6t – 290 | 250 | | ns | |
| t _{PD} | Output Data Hold | 1.5t – 90 | 40 | | ns | |
| t _{PP} | PROG Pulse Width | 10.5t – 250 | 700 | | ns | |
| t _{PL} | Port 2 I/O Setup to ALE | 4t – 200 | 160 | | ns | |
| t _{LP} | Port 2 I/O Hold to ALE | 0.5t – 30 | 15 | | ns | |
| t _{PV} | Port Output from ALE | 4.5t + 100 | | 510 | ns | |
| t _{OPRR} | T0 Rep Rate | 3t | 270 | | ns | |
| t _{CY} | Cycle Time | 15t | 1.36 | 15.0 | μs | |

NOTES:

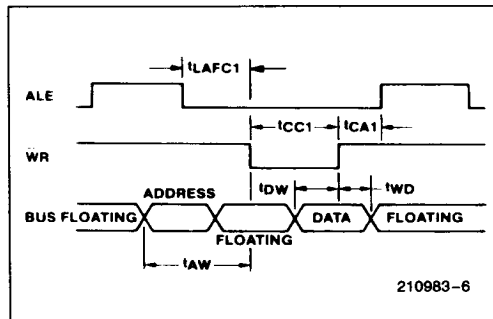
- Control outputs CL = 80 pF; BUS outputs CL = 150 pF.
- BUS High Impedance Load 20 pF.
- f(t) assumes 50% duty cycle on X1, X2. Max clock period is for a 1 MHz crystal input.

WAVEFORMS

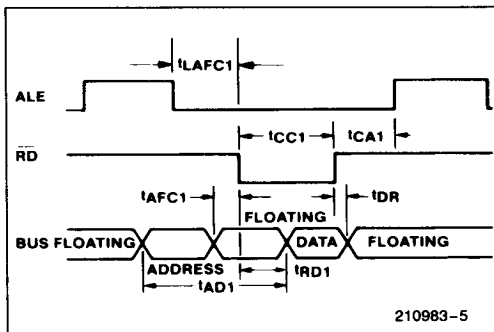
INSTRUCTION FETCH FROM PROGRAM MEMORY



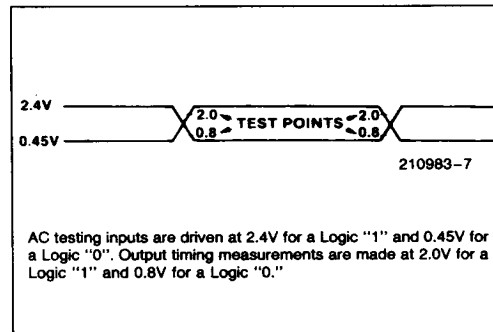
WRITE TO EXTERNAL DATA MEMORY



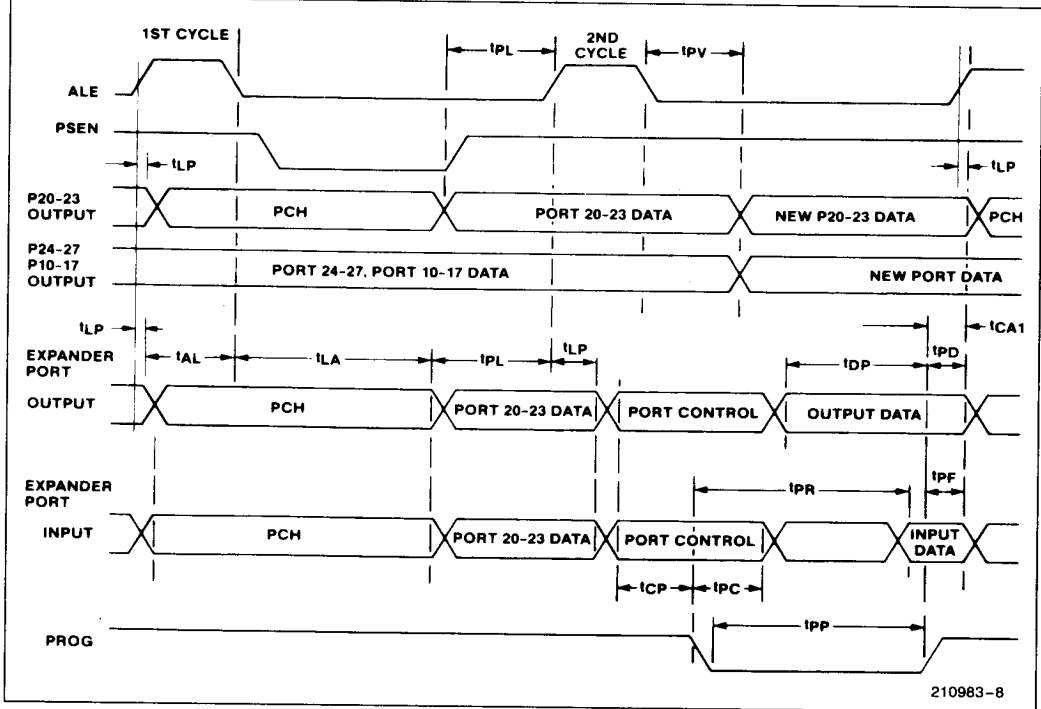
READ FROM EXTERNAL DATA MEMORY



INPUT AND OUTPUT FOR AC TESTS

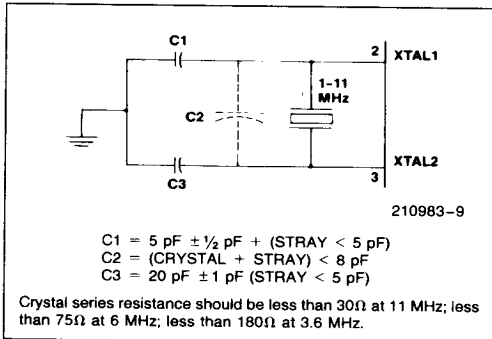


PORT 1/PORT 2 TIMING

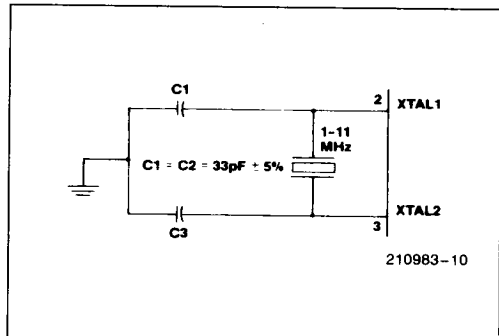


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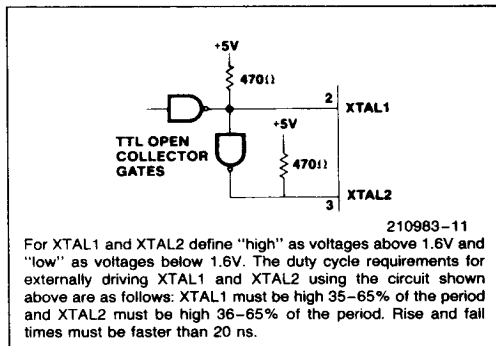
CRYSTAL OSCILLATOR MODE



CERAMIC RESONATOR MODE



DRIVING FROM EXTERNAL SOURCE



PROGRAMMING, VERIFYING AND ERASING THE 8749H (8748H) EPROM

Programming Verification

In brief, the programming process consists of: activating the program mode, applying an address, latching the address, applying data, and applying a programming pulse. Each word is programmed completely before moving on to the next and is followed by a verification step. The following is a list of the pins used for programming and a description of their functions:

| Pin | Function |
|-----------------|-------------------------------------|
| XTAL 1 | Clock Input (3 to 4.0 MHz) |
| XTAL 2 | |
| RESET | Initialization and Address Latching |
| TEST 0 | Selection of Program or Verify Mode |
| EA | Activation of Program/Verify Modes |
| BUS | Address and Data Input |
| | Data Output During Verify |
| P20–P22 | Address Input |
| V _{DD} | Programming Power Supply |
| PROG | Program Pulse Input |

WARNING

An attempt to program a missocketed 8749H (8748H) will result in severe damage to the part. An indication of a properly socketed part is the appearance of the ALE clock output. The lack of this clock may be used to disable the programmer.

The Program/Verify sequence is:

- 1) V_{DD} = 5V, Clock applied or internal oscillator operating. RESET = 0V, TEST 0 = 5V, EA = 5V, BUS and PROG floating. P10 and P11 must be tied to ground.
- 2) Insert 8749H (8748H) in programming socket.
- 3) TEST 0 = 0V (select program mode)
- 4) EA = 18V (activate program mode)
- 5) Address applied to BUS and P20–22
- 6) RESET = 5V (latch address)
- 7) Data applied to BUS
- 8) V_{DD} = 21V (programming power)
- 9) PROG = V_{CC} or float followed by one 50 ms pulse to 18V
- 10) V_{DD} = 5V
- 11) TEST 0 = 5V (verify mode)
- 12) Read and verify data on BUS
- 13) TEST 0 = 0V
- 14) RESET = 0V and repeat from step 5
- 15) Programmer should be at conditions of step 1 when 8749H (8748H) is removed from socket.

AC TIMING SPECIFICATION FOR PROGRAMMING 8748H/8749H

 $T_A = 25^{\circ}\text{C} \pm 5^{\circ}\text{C}; V_{CC} = 5\text{V} \pm 5\%; V_{DD} = 21\text{V} \pm 0.5\text{V}$

| Symbol | Parameter | Min | Max | Unit | Test Conditions |
|------------|--|-----------|-----------|---------------|-----------------|
| t_{AW} | Address Setup Time to $\overline{\text{RESET}} \uparrow$ | $4t_{CY}$ | | | |
| t_{WA} | Address Hold Time after $\overline{\text{RESET}} \uparrow$ | $4t_{CY}$ | | | |
| t_{DW} | Data in Setup Time to PROG \uparrow | $4t_{CY}$ | | | |
| t_{WD} | Data in Hold Time after PROG \downarrow | $4t_{CY}$ | | | |
| t_{PH} | $\overline{\text{RESET}}$ Hold Time to Verify | $4t_{CY}$ | | | |
| t_{VDDW} | V_{DD} Hold Time before PROG \uparrow | 0 | 1.0 | ms | |
| t_{VDDH} | V_{DD} Hold Time after PROG \downarrow | 0 | 1.0 | ms | |
| t_{PW} | Program Pulse Width | 50 | 60 | ms | |
| t_{TW} | TEST 0 Setup Time for Program Mode | $4t_{CY}$ | | | |
| t_{WT} | TEST 0 Hold Time after Program Mode | $4t_{CY}$ | | | |
| t_{DO} | TEST 0 to Data Out Delay | | $4t_{CY}$ | | |
| t_{WW} | $\overline{\text{RESET}}$ Pulse Width to Latch Address | $4t_{CY}$ | | | |
| t_r, t_f | V_{DD} and PROG Rise and Fall Times | 0.5 | 100 | μs | |
| t_{CY} | CPU Operation Cycle Time | 3.75 | 5 | μs | |
| t_{RE} | $\overline{\text{RESET}}$ Setup Time before EA \uparrow | $4t_{CY}$ | | | |

NOTE:

If TEST 0 is high, t_{DO} can be triggered by $\overline{\text{RESET}} \uparrow$.

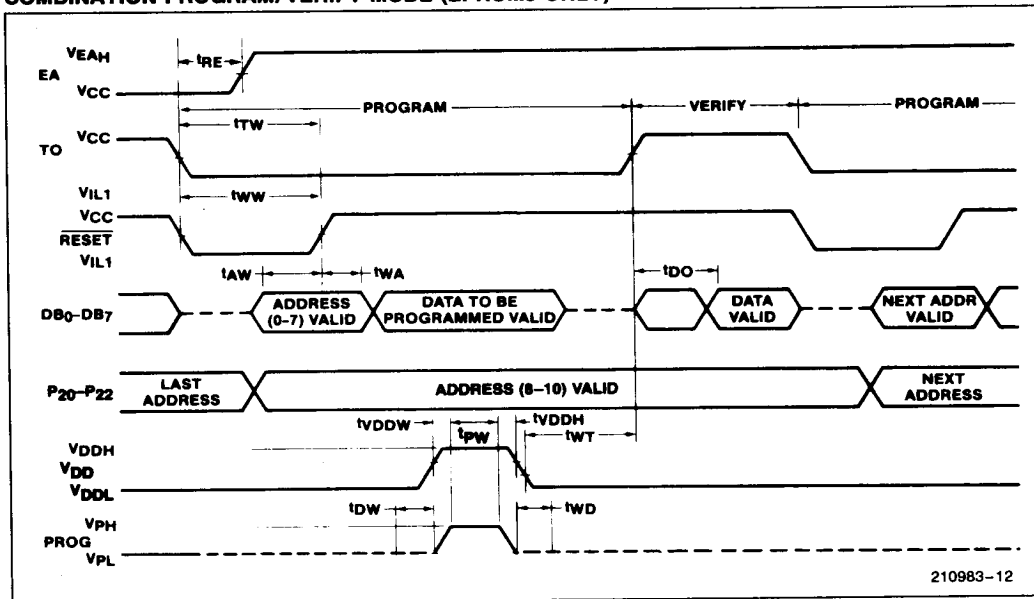
DC SPECIFICATION FOR PROGRAMMING 8748H/8749H

 $T_A = 25^{\circ}\text{C} \pm 5^{\circ}\text{C}; V_{CC} = 5\text{V} \pm 5\%; V_{DD} = 21\text{V} \pm 0.5\text{V}$

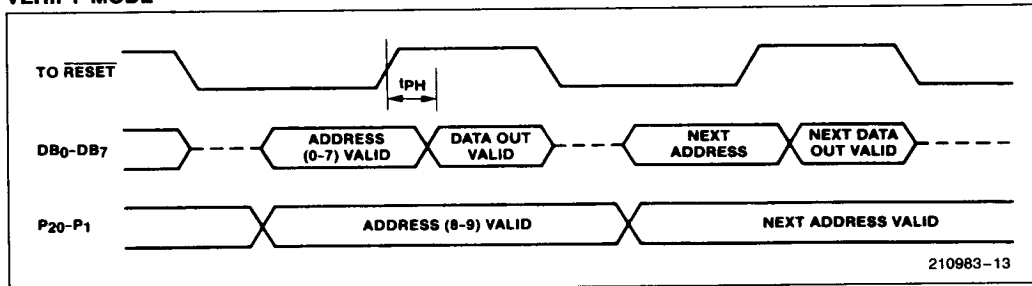
| Symbol | Parameter | Min | Max | Unit | Test Conditions |
|------------|---|------|----------|------|-----------------|
| V_{DDH} | V_{DD} Program Voltage High Level | 20.5 | 21.5 | V | |
| V_{DDL} | V_{DD} Voltage Low Level | 4.75 | 5.25 | V | |
| V_{PH} | PROG Program Voltage High Level | 17.5 | 18.5 | V | |
| V_{PL} | PROG Voltage Low Level | 4.0 | V_{CC} | V | |
| V_{EAH} | EA Program or Verify Voltage High Level | 17.5 | 18.5 | V | |
| I_{DD} | V_{DD} High Voltage Supply Current | | 20.0 | mA | |
| I_{PROG} | PROG High Voltage Supply Current | | 1.0 | mA | |
| I_{EA} | EA High Voltage Supply Current | | 1.0 | mA | |

WAVEFORMS

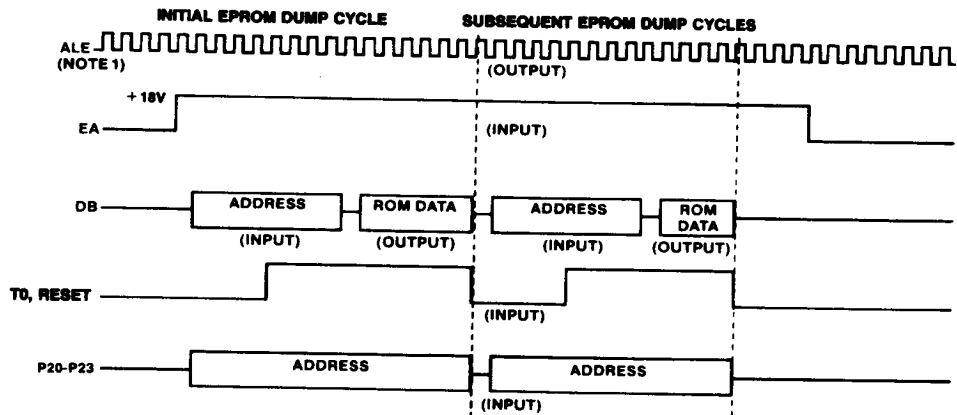
COMBINATION PROGRAM/VERIFY MODE (EPROMs ONLY)



VERIFY MODE



SUGGESTED EPROM VERIFICATION ALGORITHM FOR HMOS-E DEVICE ONLY



| | 48H | 49H |
|-----|-----|------|
| A10 | 0 | ADDR |
| A11 | 0 | 0 |

$V_{CC} = V_{DD} = +5V$
 $V_{SS} = 0V$

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NOTE:

ALE is function of X1, X2 inputs.

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